Transactions in Relaxed Memory Architectures

Brijesh Dongol Radha Jagadeesan James Riely

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- … assuming memory is *sequentially consistent* (SC)
- What about *relaxed* memory?

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- Nontransactional code?
  - Natural formalization of isolated and relaxed

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    - Coherence $\mathrm{W}x1 \xrightarrow{\text{co}} \mathrm{W}x2$ e.g., `x:=1`$\|$`x:=2`

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    - Coherence $\mathrm{W}x1 \xrightarrow{\text{co}} \mathrm{W}x2$ e.g., `x:=1`‖`x:=2`
  - Architecture generated
    - Preserved program order For SC: $\text{ppo} = \text{po}$
      For TSO: $\text{ppo} = \text{po} \setminus \text{WR}$

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- Load buffering example: Forbidden under SC, where ppo = po

Initially: `x=y=0`

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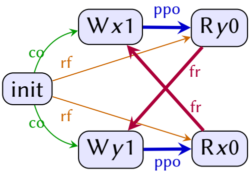

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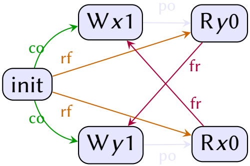

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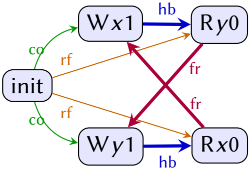

- Allowed under TSO, where ppo = po \ WR
- To get a cycle under TSO, add fences

A simple idea

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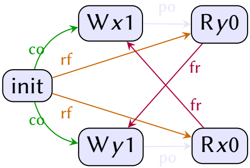

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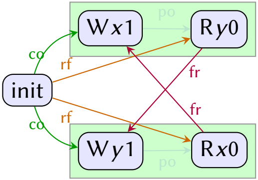

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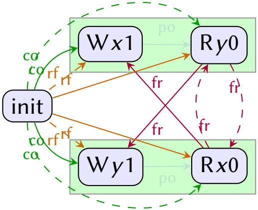

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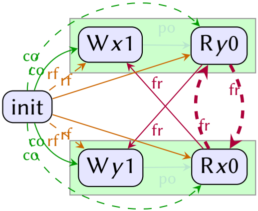

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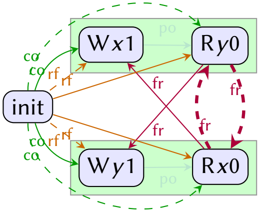

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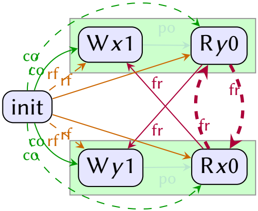

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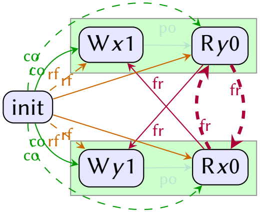

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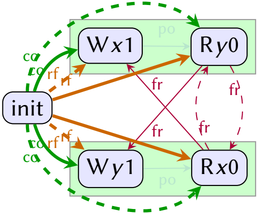

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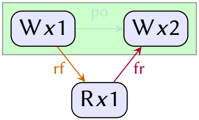
  - Ignores real time
  - Erase empty transactions, singletons
  - Lift includes nontransactional ⇒ Strong isolation

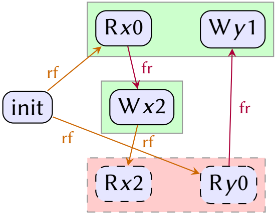
Some goals

- Nested transactions
- Weak isolation (Example under TSO)



✗ strong ✓ weak

- Abort models (Example under TSO)



✗ opaque ✓ non-opaque

Definition

- Execution is correct if AMT valid with lifted relations

- $e \xrightarrow{\text{lift(o)}} d$ when either
  1. $e \xrightarrow{\text{o}} d$
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  - Opacity: aborteds ordered w.r.t. committeds $\Rightarrow$ No changed to lift

Definition

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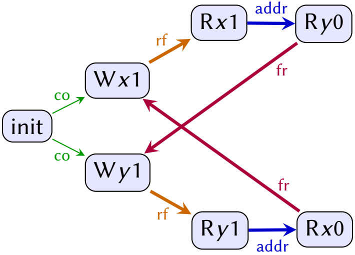
- What about standard serializability?

Standard Serializability?

- Independent Reads of Independent Writes (IRIW)
  Forbidden for *Multi-copy atomic*, e.g. SC, TSO, ARMv8



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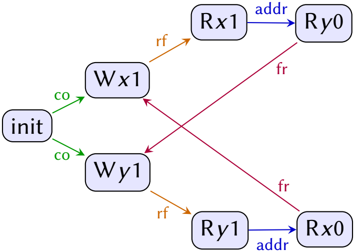

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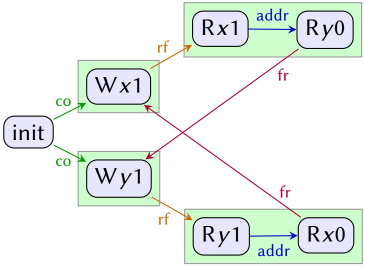

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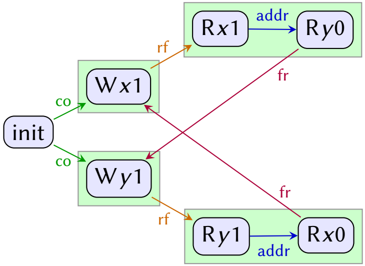

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- Lift $\Rightarrow$ Standard serializability, for multi-copy atomic
  Formalized using *Global Happens Before* [Alglave 2010]

NonOpaque Aborts

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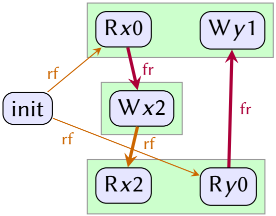

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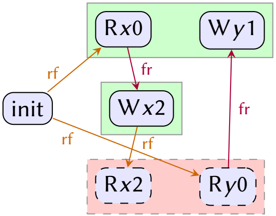

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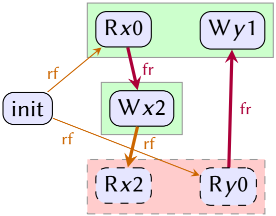

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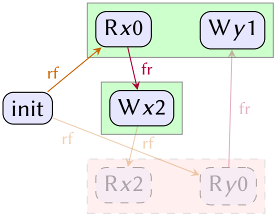

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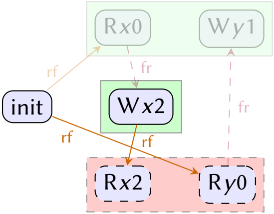

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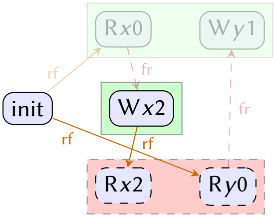

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- New formal footing for weaker conditions, e.g. VWC and TMS1

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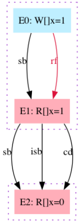

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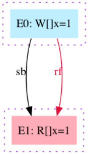

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  - Otherwise, our model strictly more expressive
    - HW enforces coherence with aborted
    - HW places fences before/after each transaction

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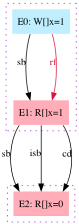

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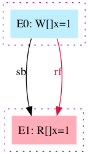

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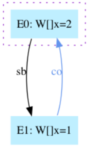

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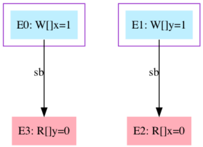

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- Our contribution: High-level view of low-level model